REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 1-6 and 9-11 are now pending with claims 1 and 9 being independent.

Claim 1 describes a method of performing a product operation with rounding in a microprocessor in response to a single rounding multiplication instruction. The method includes fetching a first pair of elements and a second pair of elements. The method also includes forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. The method further includes combining the most significant product with the least significant product to form a combined product, wherein combining comprises shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. The method also comprises rounding the combined product to form an intermediate result and shifting the intermediate result a selected amount to form a final result.

Claim 9 describes a digital system having a microprocessor that can execute a rounding multiplication instruction. The microprocessor includes storage circuitry for holding pairs of elements. A multiply circuit in the microprocessor connects to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the multiplication instruction, the multiply circuit comprising a plurality of multipliers. The microprocessor also includes an arithmetic circuit connected to receive a most significant product and a least significant product from the plurality of multipliers. The arithmetic circuit shifts the most significant product by a number of bits prior to adding the most significant product to the least significant product, the arithmetic circuit having a provision for mid-position rounding responsive to the rounding multiplication instruction. The microprocessor comprises a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding multiplication instructions.

Claims 1-6 and 9-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murakami et al. (5,442,799) in view of either Balkanski et al. (5,253,078) or Saishi et al. (6,167,419). Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. Furthermore, none of the references describes or suggests combining the most significant product with the least significant product to form a combined product.

Murakami, in relevant part, describes in the Abstract reducing the amount of calculation for determining motion compensation. Murakami in Figure 28 shows a multiplier circuit of a digital signal processor. Registers A and B are each divided into a lower n-bit section and an upper n-bit section as shown at the bottom of Figures 29(a) and 29(b). Thus, register A has a lower n-bit section A0 and an upper n-bit section A1. Register B has a lower n-bit section B0 and an upper n-bit section B1. MPY 1 shown in Figure 28 receives sections B1 and A1 and multiplies the n-bits to form an 2n bit product A1 x B1. Similarly MPY2 receives sections A0 and B1 to form A0 x B1, MPY3 receives A1 and B0 to form A1 x B0, and MPY4 receives A0 and B0 to form A0 x B0. Shifter 1 is coupled to MPY1 and left shifts the multiplication result A1 x B1 by 2n-bits as shown in Figures 29(a) and 29(b). Similarly, Shifter 2 is coupled to MPY2 and left shifts the multiplication result A0 x B1 by n-bits. Shifter 3 is coupled to MPY3 and left shifts the multiplication result A1 x B0 by n-bits. Shifter 4 is coupled to MPY4 and left shifts the multiplication result A0 x B0 by 0 bits as shown in Figures 29(a) and 29(b). Adder unit AU1 receives as input [Shifted Left 2n (A1 x B1)] and [Shifted Left 0 (A0 x B0)] and outputs (A1 x B1) + (A0 x B0). Similarly adder unit AU2 generates output (A1 x B0) + (A0 x B1). Murakami does not describe or suggest combining the most significant product with the least significant product to form a combined product. Murakami also does not describe or suggest adding the most significant product to the least significant product. Applicant's Figure 6a shows multiplying a first pair of elements to form a most significant product A1 x B1 and a second pair of elements to form a least significant product A1 x B0. The most significant product A1 x B1 is shifted left by 16 bits. The most significant product is then combined with the least significant product. As recited in Applicant's claim 1, combining comprises adding the

most significant product to the least significant product, (A1 x B1) + (A1 x B0). Murakami describes adder unit AU1 generating output (A1 x B1) + (A0 x B0) and adder unit AU2 generating output (A1 x B0) + (A0 x B1). Thus, Murakami does not describe or suggest combining the most significant product with the least significant product to form a combined product (A1 x B1) + (A1 x B0), combining comprising adding the most significant product to the least significant product. In Figure 29(b) of Murakami, the output of adder unit AU1 at 0.5 machine cycle is shown generating product (A1 x B1) + (A0 x B0).

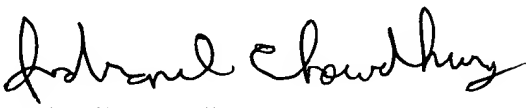
Balkanski fails to remedy the failure of Murakami to describe or suggest combining the most significant product with the least significant product to form a combined product, combining comprising adding the most significant product to the least significant product. Balkanski teaches a digital video compression system and an apparatus implementing this system. Column 9 describes a 16-bit by 16-bit multiplier for multiplying the 16-bit inputs to generate a 32-bit result. The number represented by bits 31 through 15 is rounded up by adding a 1 at bit position 14. Balkanski does not describe or suggest combining the most significant product with the least significant product to form a combined product, combining comprising adding the most significant product to the least significant product.

Saishi fails to remedy the failure of Murakami to describe or suggest combining the most significant product with the least significant product to form a combined product, combining comprising adding the most significant product to the least significant product. Saishi teaches a multiplication method and a multiplication circuit, wherein a multiplicand is multiplied by a multiplier using a multiplication process, the result of the multiplication is added by an addition process to a rounding signal to be output from a rounding signal generation process, and the result of the addition, i.e., a multiplication result obtained after rounding, is stored in a register. Saishi does not describe or suggest combining comprising adding the most significant product to the least significant product. For at least the reasons given above, Applicant respectfully submits that claims 1 and 9 are patentable over Murakami, Balkanski, and Saishi.

Claims 2-6 and 10-11 depend from independent claims 1 and 9, respectively. Accordingly, Applicant requests reconsideration and withdrawal of the rejections for claims 2-6 and 10-11 for the reasons discussed above with respect to claims 1 and 9.

In view of these remarks and amendments, Applicant submits that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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